Computer Architecture

Assignment 9

Notes: You are not asked to submit this assignment, and you can find the answer here

1. (5 points**) An ISA supports an 8-bit, byte-addressable virtual address space. The corresponding physical memory has only 128 bytes. Each page contains 16 bytes. A simple, one-level translation scheme is used and the page table resides in physical memory. The initial contents of the frames of physical memory are shown below.**

Frame Number	Frame Contents
0	Empty
1	Page 13
2	Page 5
3	Page 2
4	Empty
5	Page 0
6	Empty
7	Page Table

A three-entry translation lookaside buffer that uses Least Recently-Used (LRU) replacement is added to this system. Initially, this TLB contains the entries for pages 0, 2, and 13. For the following sequence of references, put a circle around those that generate a TLB hit and put a rectangle around those that generate a page fault. What is the hit rate of the TLB for this sequence of references? (Note: LRU policy is used to select pages for replacement in physical memory.)

References (to pages): 0, 13, 5, 2, 14, 14, 13, 6, 6, 13, 15, 14, 15, 13, 4, 3.

a. At the end of this sequence, what three entries are contained in the TLB?

b. What are the contents of the 8 physical frames?

1. (5 points**) Answer the following questions:**

a. What is the purpose of the “reference” or “accessed” bit in a page table entry?

b. Describe what you would do if you did not have a reference bit in the PTE. Justify your reasoning

c. and/or design choice.

d. What is the purpose of the dirty or modified bit in a page table entry?

e. Describe what you would do if you did not have a modified bit in the PTE. Justify your reasoning and/or design choice.