Computer Architecture, 3rd year	Suez Canal University
Midterm exam	Faculty of Computers and Informatics
Time: 60 min.	Computer Science department
7th April 2015	Dr. Ahmed Sallam

Section: ---------- الأسم: ----------

"This exam in 3 pages, make sure to answer all the questions."

1. (10 Points) **True or False?**

a. SRAM requires the data to be refreshed periodically to retain the data, while DRAM doesn't. [F]

b. SDRAM, DDRAM, and RDRAM all are new forms of SRAM. [F]

c. Major instruction set architecture (ISA) today use Dataflow model. [F]

d. Opcodes, Addressing Modes, and Data Types belong to the Microarchitecture layer. [F]

e. Modern Intel's and AMD's x86 ISA are considered CISC and RICS at the same time. [T]

f. There is small semantic gap between the CISC ISA and the programmer [T]

g. In ISA design, Uniform instructions decode usually chosen with fixed length instructions. [T]

h. In Load/store architecture, instructions operate only on registers. [T]

i. In a Single-cycle machine, Control signals are generated in the same clock cycle as the one during which data signals are operated on. [T]

j. Using Hardwired control (combinational logic), control signals associated with an each instruction stored in a memory structure called control store. [F]

2. (4 points**) List 3 design considerations when designing a new computer architecture? What determines the importance of each design consideration?**

*** Cost, Performance, Power consumption**

*** Considerations determined by the problem (application) space, or the users/market**

2. (10 points**) Consider two machines, X and Y , described below.**

Machine X: A three-address memory/memory machine that takes two memory locations as source operands and one memory location as a destination operand. Machine X's ISA has the following characteristics:

- OP M3, M1, M2: Performs the binary operation OP on the values stored at memory locations M1 and M2 and stores the result back into memory location M3 (M3 ← M1 OP M2).
- OP M3, M1, Immediate: Performs a binary operation OP on the value stored at memory location M1 and value Immediate and stores the result back into memory location M3 (M3 ← M1 OP Immediate).
- Opcode stored in 7 bytes and data values stored in 4 bytes.

Machine Y: A three-address load/store machine whose sources and destination are registers. Values are loaded into registers using memory operations. Machine Y 's ISA has the following characteristics:

- OP R3, R1, R2: Performs a binary operation OP on the values stored at registers R1 and R2 and stores
- the result back into register R3 (R3 ← R1 OP R2).
- OP R3, R1, Immediate: Performs a binary operation OP on the value stored at registers R1 and immediate value Immediate and stores the result back into register R3 (R3 ← R1 OP Immediate).
- LD R1, M: Loads the value at memory location M into register R1.
- ST R2, M: Stores the value in register R2 into memory location M.
- Opcode stored in 4 bytes and data values are stored in 4 bytes

Consider the following two programs:

```
Program A          Program B
A = A + 1;         A = A + B;
B = B + 2;         B = A + B;
C = C - 3;         C = B - A;
```

a. For each of the two programs, A and B, write the corresponding assembly code for each of the two machines, X and Y. For Machine Y, ensure to (i) reuse the register values whenever possible. (ii) store the register values back into memory after executing all the code.

Machine X		**Machine Y**	
Program A	Program B	Program A	Program B
Add A, A, 1=7(Instruction)+ 4(A)+4(b)	Add A,A,B= 7(inst.)+4(A)+4(B)+4(WB A)	LD R1, A =4(Instruction)+4(A)	LD R1, A =4(Instruction)+4(A)
Add B, B, 2 =7+2*4	Add B,A,B= 7+3*4	Add R1,R1,1 =4+0	LD R2, B =4(Instruction)+4(A)
Sub C, C, 3= 7+2*4	Sub C,B,A= 7+3*4	LD R2, B =4+4	ADD R1,R1,R2=4+0
		Add R2,R2,2 =4+0	ADD R2,R2,R1=4+0
		LD R3, C =4+4	SUB R3,R2,R1=4+0
		SUB R3,R3,3 =4+0	ST R1, A =4+4
		ST R1, A =4+4	ST R2, B =4+4
		ST R2, B =4+4	ST R3,C =4+4
		ST R3, C =4+4	

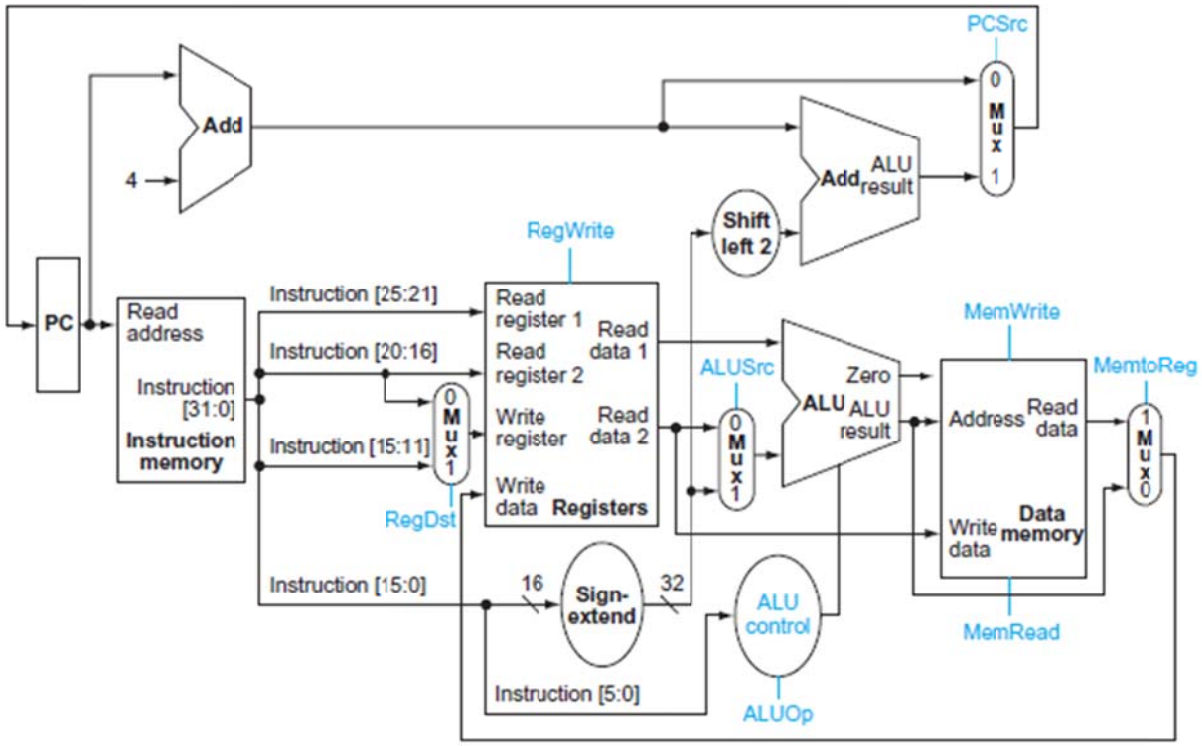
b. Compute the total number of bytes (instruction and data) transferred to/from memory for each of the two programs, A and B, for each of the two machines, X and Y .

	Program A	Program B
Machine X	45	57
Machine Y	60	52

c. Between machines X and Y , (i) does the machine that transfers the smaller total number of bytes for Program A also transfer the smaller total number of bytes for Program B? (ii) If yes, explain why this is the case; otherwise, explain why there is a difference.

Answer: **No, because Machine X need to transfer A,B,C to/from memory in both programs, while Machine Y can reuse the registers whenever it's possible.**

3. (6 points**) Consider the following figure to answer the questions in the next page:**



For the Instructions:

i. `OR Rd,Rs,Rt` → Interpretation: `Reg[Rd] = Reg[Rs] OR Reg[Rt]`

ii. `ADDi Rt,Rs,IMM` → Interpretation: `Reg[Rt]= Reg[Rs] + IMM`

a. What are the values of control signals generated by the control in for the above instruction? (Use 1, 0 or X "Don't Care")

	RegDst	RegWrite	ALUOp	ALUSrc	MemWrite	MemRead	MemtoReg	PCSrc
i	0	1	'OR' or 1 (mux)	0	0	0	0	0 or X
ii	1	1	Add or 1 (mux)	1	0	0	0	0 or X

b. Select resources (blocks) that perform a useful function for these instructions:

	Instruction Memory	Registers	ALU	Data memory	Branch ALU	PC Adder
i	☑	☑	☑	☐	☐	☑
ii	☑	☑	☑	☐	☐	☑

c. Select resources (blocks) that produce outputs, but their outputs are not used for these instructions

	Instruction Memory	Registers	ALU	Data memory	Branch ALU	PC Adder
i	☐	☐	☐	☐	☑	☐
ii	☐	☐	☐	☐	☑	☐

Do your best, Good Luck