Computer Architecture

Assignment 4

Due: Next section. (*one day before if you submit by email***)**

Notes: This assignment is individual assignment, every student should complete by himself.

1. (5 points **) True or false**

a. In Load/store architecture, operate instructions operate only on registers.

b. RISC ISA usually implement many address modes.

c. x86 architecture store each instruction in 32 bits.

d. 0-address machine usually called queue machine.

e. 0-address machine is better than 2-address machine.

f. All ISAs provide double linked list as a primitive data type.

g. ISAs with fewer number of data types are easier for programmers

h. Registers are a set of small storage places within the processor.

i. Most ISAs provide registers with a size range between 1 MB and 5 MB.

j. More registers can decrease processor performance and by preventing data locality.

k. Instructions can be divided into different classes include operate instruction, data movement instructions, control flow instructions.

2. (5 points**) The following assembly programs implement Fibonacci sequence in x86 and ARM:**

a. **x86**	b. **ARM**

`.data`
`n byte 5`
`.code`
`main PROC`
`mov eax, 1`
`movzx ecx, n`
`startLoop:`
`mul ecx`
`loop startLoop`
 	
`main ENDP`
`END main`
	`.global main`
	`.text`
	`main:`
	`MOV R2, #5 ;Init the character`
	`MOV R1, #1`
	`loop:`
	`MOV R3,R1`
	`MUL R1,R3,R2`
	
	`SUB R2, R2, #1 ;Increment it`
	`CMP R2, #1 ;Check the limit`
	`BGE loop`

a. Refer to this x86 timing manual and calculate number of cycles for program "a" if compiled with Intel Core 2 -L32 and AMD-k10

b. Refer to this ARM timing manual and calculate number of cycles for program "b" if compiled with Cortex-M3.

c. Conclude the difference between the results of question 4.a and 4.b.