Computer Architecture

Assignment 9

Due: Next section. (*one day before if you submit by email***)**

Notes: This assignment is individual assignment, every student should complete by himself.

1. (5 Points**) True or False? Why?:**

a. The main goal of Pipelining is to reduce the cost.
b. Output dependence and Anti dependence is not a real data dependences.
c. Ideal pipelining requires uniform suboperations.
d. MIPs processor architecture use scoreboarding interlocking technique to detect and eliminate the dependences.
e. Resources contention problem has no visible solution yet.

2. (5 Points**) Assume the 5 stages of 2 processors have the following latencies:**

	Fetch	Decode	Execute	Memory	WriteBack
a.	300 ps	400 ps	350 ps	550 ps	100 ps
b.	200 ps	150 ps	100 ps	190 ps	140 ps

Note: Assume that when pipelining, each pipeline stage costs 20ps extra for the registers between pipeline stages.

2.1 In a non-pipelined processor: what is the cycle time? What is the latency of an instruction? What is the throughput?

2.2 In a Pipelined processor: What is the cycle time? What is the latency of an instruction? What is the throughput?

2.3 If you could split one of the pipeline stages into 2 equal halves, which one would you choose? What is the new cycle time? What is the new latency? What is the new throughput?

2.4 What is the required conditions to perform an ideal pipelining for the second processor.

3. (5 Points**)** Consider two machines, X and Y , described below.

Machine X: A three-address memory/memory machine that takes two memory locations as source operands and one memory location as a destination operand. Machine X's ISA has the following characteristics:

- OP M3, M1, M2: Performs the binary operation OP on the values stored at memory locations M1 and M2 and stores the result back into memory location M3 (M3 ← M1 OP M2).
- OP M3, M1, Immediate: Performs a binary operation OP on the value stored at memory location M1 and value Immediate and stores the result back into memory location M3 (M3 ← M1 OP Immediate).
- Opcode stored in 7 bytes and data values stored in 4 bytes.

Machine Y: A three-address load/store machine whose sources and destination are registers. Values are loaded into registers using memory operations. Machine Y 's ISA has the following characteristics:

- OP R3, R1, R2: Performs a binary operation OP on the values stored at registers R1 and R2 and stores
- the result back into register R3 (R3 ← R1 OP R2).
- OP R3, R1, Immediate: Performs a binary operation OP on the value stored at registers R1 and immediate value Immediate and stores the result back into register R3 (R3 ← R1 OP Immediate).
- LD R1, M: Loads the value at memory location M into register R1.
- ST R2, M: Stores the value in register R2 into memory location M.
- Opcode stored in 4 bytes and data values are stored in 4 bytes

Consider the following two programs:

```
Program A          Program B
A = A + 1;         A = A + B;
B = B + 2;         B = A + B;
C = C - 3;         C = B - A;
```

a. For each of the two programs, A and B, write the corresponding assembly code for each of the two machines, X and Y. For Machine Y, ensure to (i) reuse the register values whenever possible. (ii) store the register values back into memory after executing all the code.

Machine X		**Machine Y**	
Program A	Program B	Program A	Program B

b. Compute the total number of bytes (instruction and data) transferred to/from memory for each of the two programs, A and B, for each of the two machines, X and Y .

	Program A	Program B
Machine X		
Machine Y		

Between machines X and Y , (i) does the machine that transfers the smaller total number of bytes for Program A also transfer the smaller total number of bytes for Program B? (ii) If yes, explain why this is the case; otherwise, explain why there is a difference.