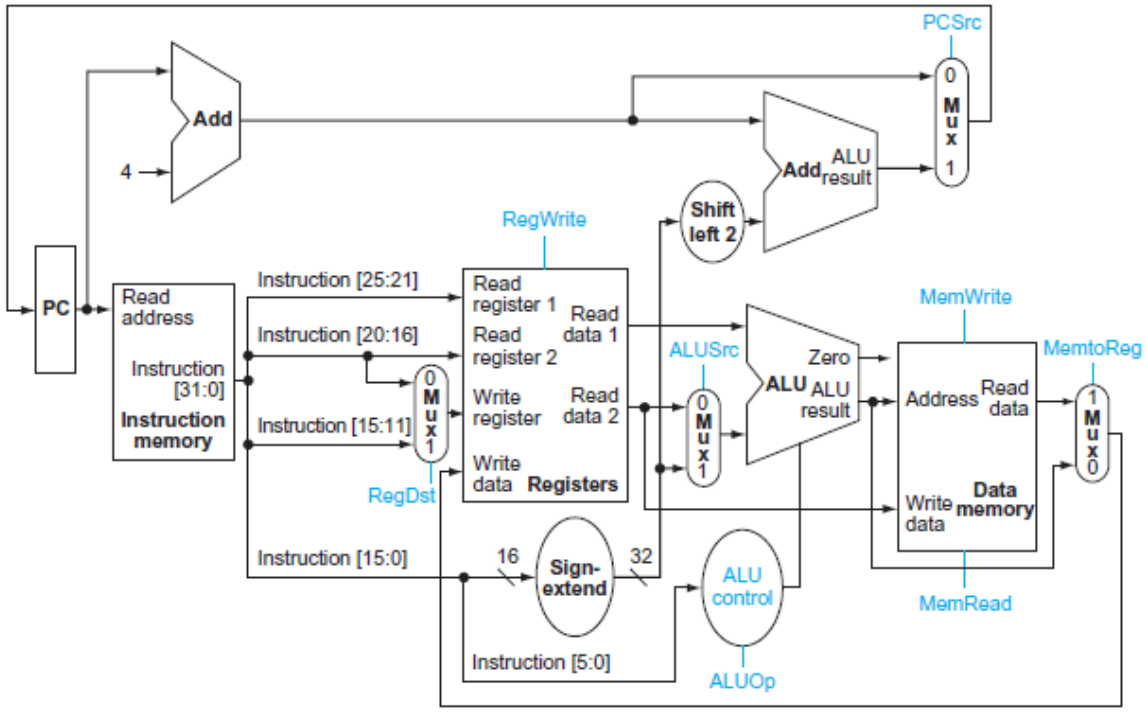
Computer Architecture

Assignment 7

Due: Next section. (*one day before if you submit by email***)**

Notes: This assignment is individual assignment, every student should complete by himself.

Consider the following figure to answer the questions: (*For help refer to P&H Ch 4***)**



1. **(**5 Points**) For Instruction:**

   `AND Rd,Rs,Rt` => Interpretation: `Reg[Rd]= Reg[Rs] AND Reg[Rt]`

   What are the values of control signals generated by the control in for the above instruction?

2. **(**5 Points**)** For Instruction:

   `LWI Rt,Rd(Rs)` => Interpretation: `Reg[Rt] = Mem[Reg[Rd]+Reg[Rs]]`

   a. Which existing blocks (if any) can be used for this instruction?

   b. Which new blocks (if any) do we need for this instruction?

   c. What new signals do we need (if any) from the control unit to support this instruction?

3. (5 Points**) When processor designers consider a possible improvement to the processor datapath, the decision usually depends on the cost/performance trade-off . In the following three problems, assume that we are starting with a datapath from the previous Figure, where I-Mem, Add, Mux, ALU, Regs, D-Mem, and Control blocks have latencies of 400 ps, 100 ps, 30 ps, 120 ps, 200 ps, 350 ps, and 100 ps, respectively, and costs of 1000, 30, 10, 100, 200, 2000, and 500, respectively.**

Consider the addition of a multiplier to the ALU. This addition will add 300 ps to the latency of the ALU and will add a cost of 600 to the ALU. The result will be 5% fewer instructions executed since we will no longer need to emulate the MUL instruction.

a. What is the clock cycle time with and without this improvement?
b. What is the speedup achieved by adding this improvement?
c. Compare the cost/performance ratio with and without this improvement.